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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,197	09/15/2003	Yin-Chang Chen	AMIP0020USA	2196

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
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EXAMINER	
CUNNINGHAM, TERRY D	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,197	CHEN ET AL.	
	Examiner	Art Unit	
	Terry D. Cunningham	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

The drawings are objected to because Fig. 5 shows transistors 142, 154 and the transistor connected therebetween as having the source connected to the gate, contrary to what is stated in the specification. Due to the voltage polarity across these transistors, it is necessarily true that nodes 148 and 158 are sources, not "drains". To be consistent with the specification concerning the common gate-drain connections and for the circuit to work properly, as will be discussed below, Fig. 5 should show the gates of the transistors in element 138 as being connected to the upper terminals thereof, rather than the lower terminals.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 10-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Due to the connection shown in Fig. 5 for the transistors in element 138 and due to the voltage polarity thereacross, these transistors will always be off, contrary to what is stated in the specification. If the intent of the invention is that the transistors in element 138 operate as diodes, then it would be required that the gates of these transistors in element 138 be connected to the upper terminals thereof, rather than the lower terminal (similarly as discussed above). Further, if this is what is intended, corresponding changes in the specification would be

necessitated. For example, the "drain" and "source" references would need to be interchanged and the specification should no longer state that the common gate-drain connections are connected to the output of the "negative charge pump" 132 and the input of the "differential amplifier" 86.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 26, there is no support in the specification for element 84 of Fig. 3 being a "voltage-controlled oscillator". A "voltage-controlled oscillator" is notoriously well known in the art as being an oscillator that a variable frequency based on a received variable analog control voltage. As seen in Fig. 3 and as expressly disclosed in the specification, oscillator 84 has a fixed frequency that is turned on or off based on the output of element 88 (which effectively provides a digital output signal).

Claims 2-9 are rejected as including the indefiniteness discussed above with claim 1.

Claims 10-18 are rejected for similar reasons as claims 1-9.

In claims 10-18, it is not understood how the circuit can operate having the recited connections for the "gate" and "drain" terminals of the "serially connected NMOS transistors" for similar reasons as discussed above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seo et al. (USPN 6,518,828) in view of Chern (USPN 5,039,877). Seo et al. disclose, in Fig. 1, a circuit comprising: a "charge pump (11)"; "a level shift circuit (23)"; "a differential amplifier (22)"; and an "oscillator (CLOCK 1)". The reference to Seo et al. discloses that that the circuit of Fig. 1 provides a boosted output voltage rather than a "negative" voltage. However, it is notoriously well known, as taught in the reference to Chern, that a positive charge pump can be modified to be a "negative charge pump" by merely reversing the power supply polarity and the direction of the detection diodes. Such an arrangement would obtain the advantage disclosed by Seo et al. of low power supply sensitivity. Therefore, it would have been obvious for one skilled in the art to modify the reference to Seo et al. to be a "negative charge pump circuit" by reversing the power supply polarity and the direction of the detection diode, such as taught by Chern, to obtain the expected advantage of low power supply sensitivity in a circuit that provides a negative output voltage.

With respect to claims 1-9, the reference to Seo et al. only discloses broad diodes, rather than diode-connected PMOS transistors. However, it is notoriously well known that diodes and diode-connected PMOS transistors are art-recognized equivalents. Additionally, since the reference to Seo et al. is a MOS circuit, such an arrangement would have simple and readily accessible structure. Therefore, it would have been obvious for one skilled in the art to use

diode-connected PMOS transistors in place of the broad transistors of Seo et al. for the expected advantage of simple and readily accessible structure.

With respect to claims 10-18, the reference to Seo et al. only discloses broad diodes, rather than diode-connected NMOS transistors. However, it is notoriously well known that diodes and diode-connected PMOS transistors are art-recognized equivalents. Additionally, since the reference to Seo et al. is a MOS circuit, such an arrangement would have simple and readily accessible structure. Therefore, it would have been obvious for one skilled in the art to use diode-connected NMOS transistors in place of the broad transistors of Seo et al. for the expected advantage of simple and readily accessible structure.

Claims 3-9 and 12-18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terry Cunningham whose telephone number is 571-272-1742. The examiner can normally be reached on Monday-Thursday from 7:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Terry D. Cunningham
Primary Examiner
Art Unit 2816

TC
September 7, 2004